REMARKS

This is intended as a full and complete response to the Final Office Action dated September 15, 2006, having a shortened statutory period for response set to expire on December 15, 2006. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1, 3, 5-11, 13-20, 25-26, and 28-30 are pending in the application. Claims 1, 3, 5-11, 13-20, 25-26, and 28-30 remain pending following entry of this response.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 3, 5-6, 9-14, 16-19, 21, 23 and 25-30 are rejected under 35 U.S.C. 102(e) as being anticipated by *Snyder et al.* (US Pat. No. 6,829,190, hereinafter *Snyder*). Applicants respectfully traverse this rejection.

Cancelled Claims

With respect to claims 12, 21, 22, 23, and 27, the claims were previously cancelled. Accordingly, withdrawal of the rejection with respect to claims 12, 21, 22, 23, and 27 is respectfully requested. *See Final Office Action dated September 15, 2006,* Page 2, Item 2.

Overview of the Applicable Law

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9

USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The Cited Reference

The Examiner cites *Snyder* in rejecting the pending claims. *Snyder* relates to a method for programming a memory device, which can apply a programming voltage and programming time for a specific memory device and which can utilize the memory device temperature when calculating the programming voltage and programming time for a specific memory device. *See* Col. 2, Lines 50-59.

The Examiner's Current Rejection

As an initial matter, Applicants respectfully submit that the Examiner has not made a proper rejection with respect to each of the pending claims. As described above, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Thus, to support a rejection under 35 U.S.C. § 102(e), the prior art reference cited by the Examiner must teach each element of each rejected claim. *See id.* In the current rejection, Applicants respectfully submit that the Examiner has not mapped each claim element to a recitation in the cited reference, and further submit that the reference, in fact, does not teach each of the claimed elements. *See Final Office Action dated September 15, 2006* (hereinafter *Final Office Action*), Pg. 2, Item 2. With respect to claims 3, 5-6, 9, 11, 13-14, and 16-19, 26, 28, and 29, the Examiner has completely omitted any specific discussion of the language of the claims. For example, with respect to claims 3 and 17, the Examiner has omitted any discussion of a refresh rate. With respect to claims 5 and 13, and dependents therefrom, the Examiner has omitted any discussion of a detector and a reference. Accordingly, Applicants respectfully submit that the Examiner has not met the burden of showing that each element of each rejected claim is cited in the prior art reference. Therefore, withdrawal of the rejection is respectfully requested.

In the Examiner's current rejection, the Examiner has provided additional statements and citations indicating the Examiner's reasoning for the present rejection. In view of the Examiner's additional statements and citations, Applicants' respectfully reiterate Applicants' previously stated arguments (*See Response to Office Action dated March 31, 2006*) and further provide the following, additional arguments.

The Examiner states that *Snyder* describes a programmable voltage pump that can produce a range of programming voltages to a memory device as a function of temperature and time, citing Column 6, Lines 37-39 and Column 8, Lines 16-18 of *Snyder*. *See Final Office Action*, Pg. 2, Item 2. The Examiner states that the programmable voltage pump produces a boosted voltage VPP pump which is applied to the word lines of a memory device, citing *Snyder* at Column 11, Line 17. *See id.* The Examiner then refers to Figures 5C and 5D of *Snyder,* stating that the figures "inherently illustrate that as the temperature decreases, the programming voltage to the memory device increases".

First, Applicants note that, with respect to the cited Figure 5D, the cited figure does not depict the boosted voltage VPP (or any programming voltage) which the Examiner asserts is applied to the word lines of a memory device. This is clear in Figure 5D, which refers to VMP (and does not refer to VPP). *See Snyder,* Figure 5D. This is also clear in the text of *Snyder* which describes Figure 5D, stating that the graph "shows saturation voltage versus pulse width" (emphasis added). *Snyder,* Column 10, Lines 65-66. Thus, the cited margin voltage VMP is a saturation voltage and refers to an intrinsic property of the die (a saturation voltage) *and not a programming voltage which is internally generated.* Column 10, Line 65 – Column 11, Line 4.

Second, with respect to the Examiner's statement that Figures 5C and 5D "inherently illustrate that as the temperature decreases, the programming voltage to the memory device increases", Applicants note that such teaching is neither inherent nor explicit in *Snyder.*

With respect to the explicit teaching of *Snyder* with respect to Figure 5D, *Snyder* merely states that an "ideal pulse width can be determined based on the erase margin saturation curve for each die". Column 10, Line 65 – Column 11, Line 4. Thus, the graph depicted in Figure 5D is used in determining an ideal pulse width. *See id.*

Accordingly, the cited figure does not describe selecting a programming voltage as asserted by the Examiner. *See id.*

With respect to the Examiner's inherency argument that the cited Figures "illustrate that as the temperature decreases, the programming voltage to the memory device increases", Applicants submit that such a teaching is not inherent in *Snyder*. With respect to the law of inherency, the fact that a certain result or characteristic may occur in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). *See MPEP* Sec. 2112. To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999).

In the present case, with respect to the Examiner's suggestion that the cited Figures "inherently illustrate that as the temperature decreases, the programming voltage to the memory device increases", the Examiner has not provided any extrinsic evidence indicating why the missing descriptive matter is necessarily present in *Snyder*. For example, as described above, the cited Figures merely refer to determining an ideal pulse width based on the erase margin saturation curve. The cited Figures do not refer to a programming voltage, and the Examiner has not provided extrinsic evidence indicating why it is inherent that the Figures "illustrate that as the temperature decreases, the programming voltage to the memory device increases". Accordingly, the Examiner has met the burden of establishing that such a teaching is inherent in *Snyder*.

Therefore, the cited reference does not describe varying a level of one or more internally generated voltages based on temperature information, comprising decreasing the level of one or more internally generated voltages as device temperature increases and applying the one or more internally generated voltages to an array of memory cells of the memory device. Withdrawal of the rejection is respectfully requested.

Claim Rejections - 35 U.S.C. § 103

Claims 5-6 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Snyder*, in view of Applicant's Fig. 1 Prior Art. Also, Claims 7-8 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Snyder*, in view of Applicant's Fig.1 Prior Art and further in view of *Park et al.*, 6,958,947. In each of the present rejections under 35 U.S.C. 103(a), the Examiner relies on the rejection of the independent claims under 35 U.S.C. Sec. 102 in view of *Snyder*. Applicants respectfully submit that the rejection of the independent claims under 35 U.S.C. Sec. 102 in view of *Snyder* has been overcome as described above. Accordingly, the present rejection under 35 U.S.C. Sec. 103(a) is also believed to be overcome. Therefore, withdrawal of the rejection is respectfully requested.

Claim Rejections - Double Patenting

Claims 1, 3, 5-11, 13-20, 25-26 and 28-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-28 of U.S. Patent No. 7,009,904.

In the present rejection, the Examiner states that claims 1-24 of the pending application are not patentably distinct from the claims of U.S. Patent No. 7,009,904 because "the voltage generator as recited in claims 1-24 of the present invention is obviously the same as the voltage generator recited in claims 1-28 of U.S. Patent No. 7,009,904, since they are both drawn to the embodiments as shown in the same Figs. 2-3 and 4A-B in the present invention and in U.S. Patent No. 7,009,904". *See Final Office Action,* Pg. 7, Item 9 (emphasis added). Accordingly, the Examiner appears to argue that the claims of the pending application are not distinct from the claims of U.S. Patent No. 7,009,904 because the drawings of both applications appear similar.

Applicants respectfully submit that the Examiner's rejection of the pending claims under nonstatutory obviousness-type double patenting is incorrect because it does not apply the correct legal test for nonstatutory obviousness-type double patenting. As stated in MPEP § 804(II)(B)(1), "In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is - does any claim in the

application define an invention that is merely an obvious variation of an invention claimed in the patent?". Thus, a nonstatutory obviousness-type double patenting rejection requires examination of the claims in both cases, and not the drawings as asserted by the Examiner. This is clear from the statement in MPEP § 804(II)(B)(1) that:

Any obviousness-type double patenting rejection should make clear:

(A) The differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent. (Emphasis Added)

Because the Examiner has not provided any specific comparison of the claims on a claim-by-claim basis and element-by-element basis, Applicants submit that the Examiner has not established the requirements of a nonstatutory obviousness-type double patenting rejection. Withdrawal of the rejection is therefore respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicants respectfully submit that the claims are in condition for allowance and respectfully request that the claims be allowed.

If the Examiner believes any issues remain that prevent this application from going to issue, the Examiner is strongly encouraged to contact the undersigned attorney to discuss strategies for moving prosecution forward toward allowance.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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